CMOS-Compatible Ferroelectric Synapse Technology for Analog Neural Networks

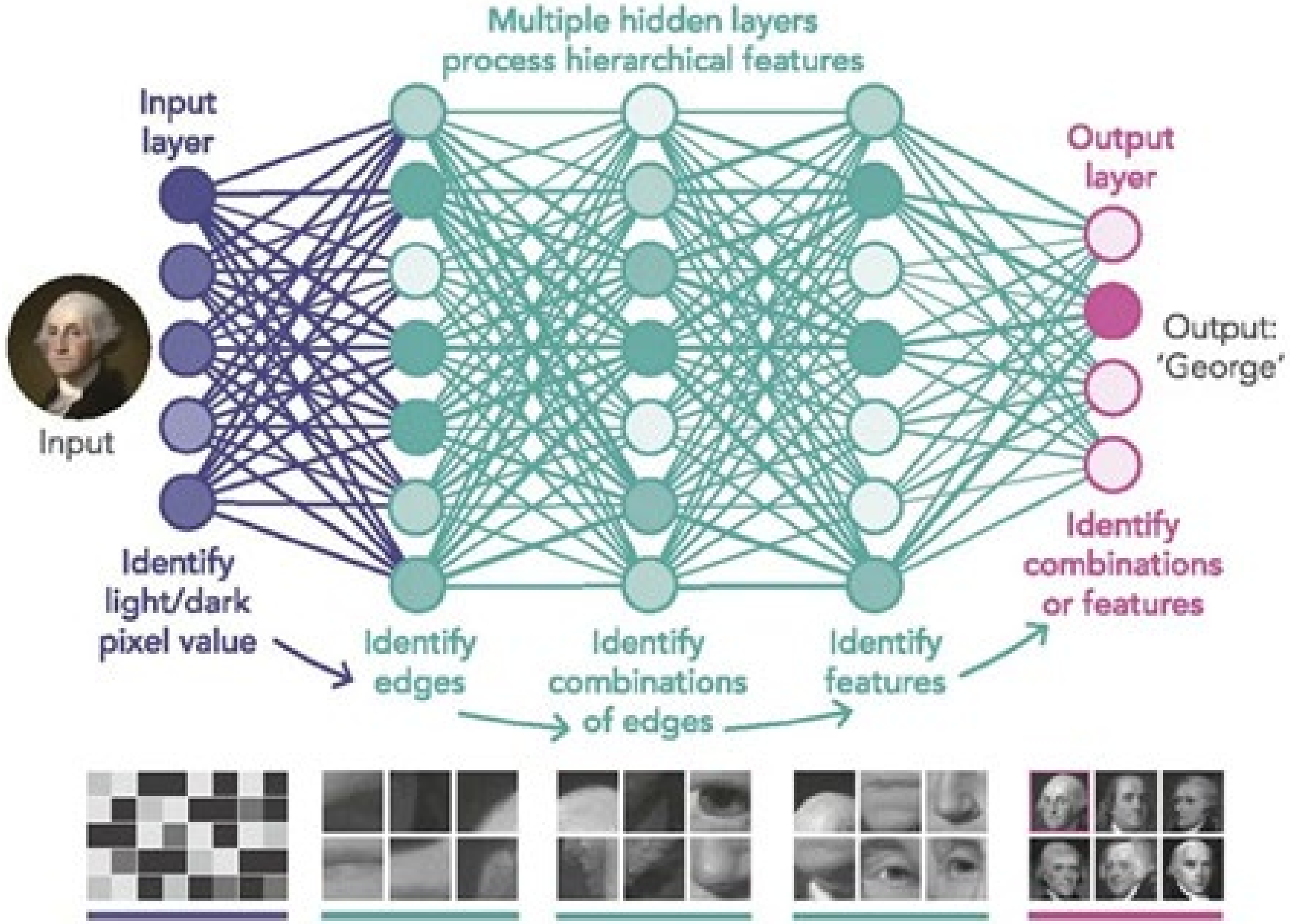
Jesús A. del Alamo, Yanjie Shao, Taekyong Kim, Elham R. Borujeny, and Dimitri A. Antoniadis

MIT

MIT AI Hardware Program Fall Research Update
MIT, October 14, 2022

Deep Learning - Neural Networks

Computation using data representations with multiple levels of abstraction



Deep Neural Networks:

- Image recognition
- Speech recognition
- Natural language processing
- Machine translation
- Bioinformatics
- Drug design
- …

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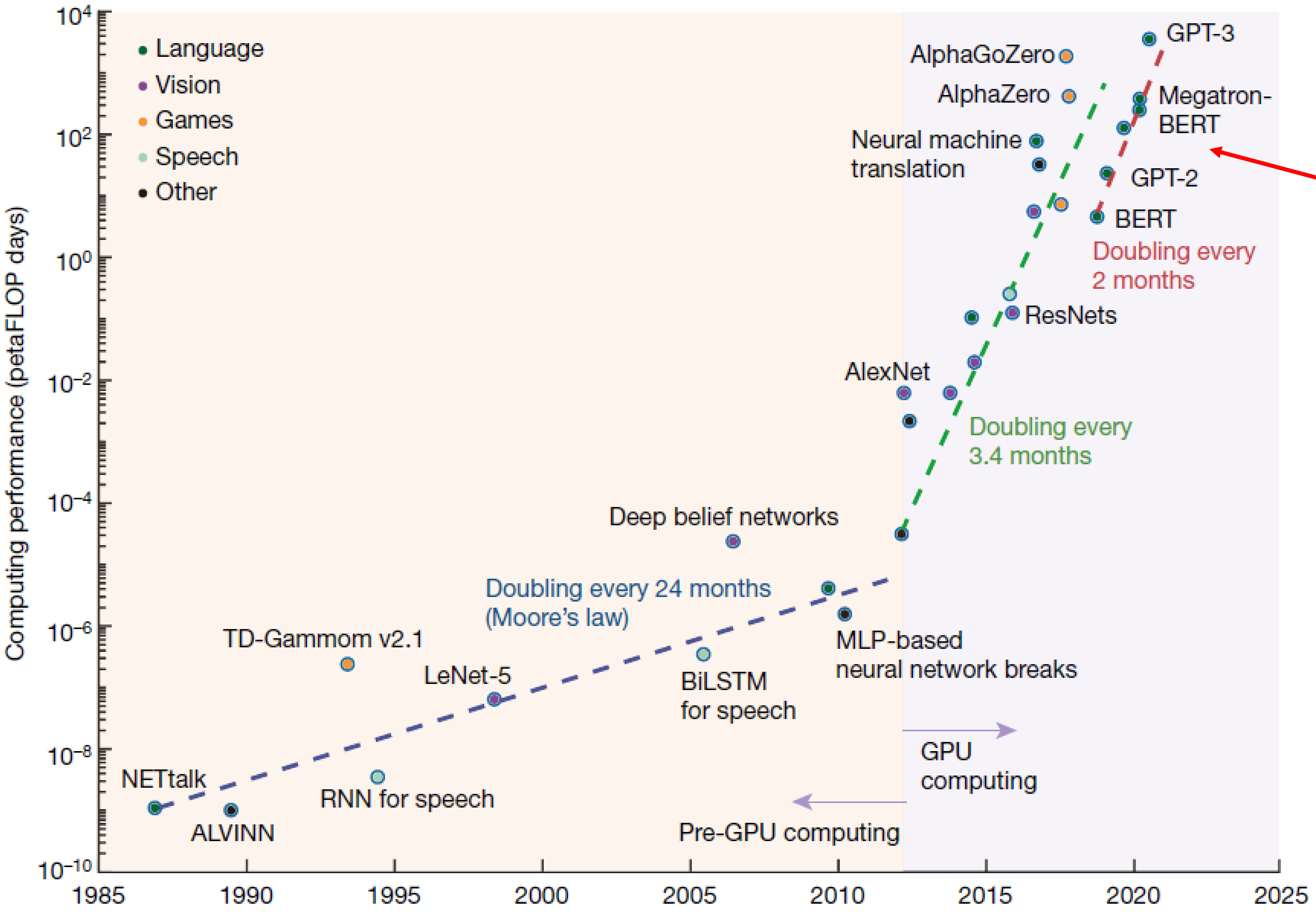
Computing Performance needs of AI



Doubling every 2 months!

Mehonic, Nature 2022

WIRED

WILL KNIGHT BUSINESS JAN 21, 2020 7:00 AM

AI Can Do Great Things—if It Doesn't Burn the Planet

The computing power required for AI landmarks, such as recognizing images and defeating humans at Go, increased 300,000-fold from 2012 to 2018.

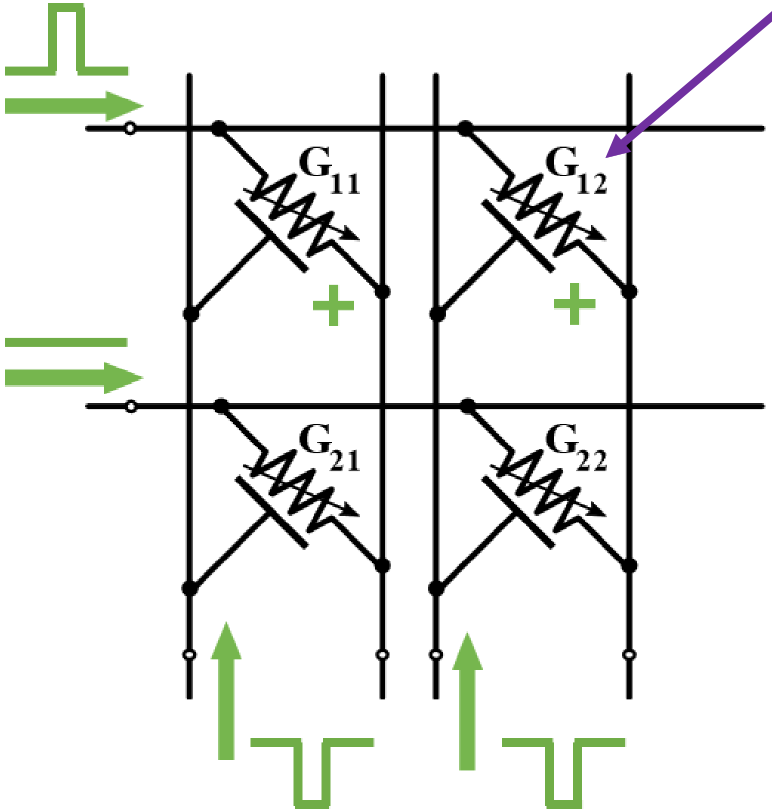
Analog Deep Neural Network

Multiply-Accumulate operation at heart of Matrix Multiplication

$$I_j = \sum_{i=1}^{N} G_{ij} V_i$$

Kirchoff's Law

Ohm's Law



Programmable non-volatile resistor

ANNs vs. Digital NNs:

- Footprint ↓
- Energy efficiency ↑↑
- Latency ↓

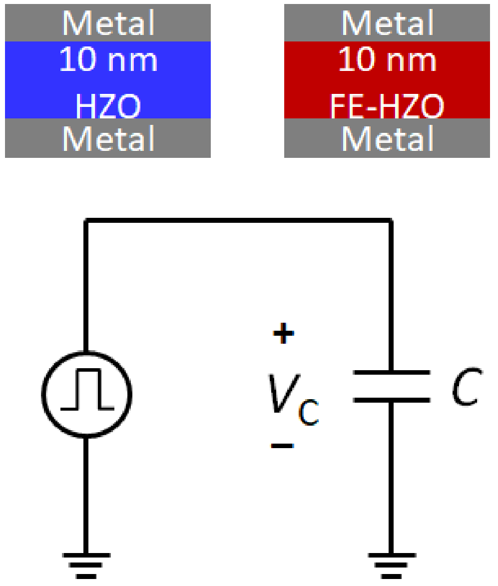
Key challenge:
device with desired characteristics does not exist today!

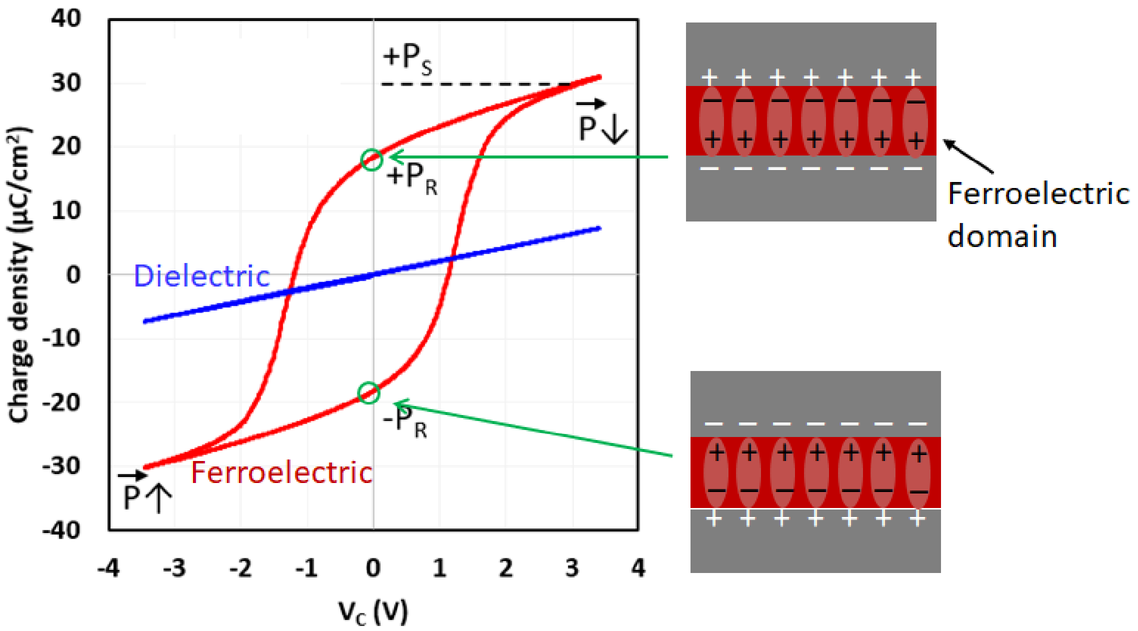
Burr, AdvPhysX 2017

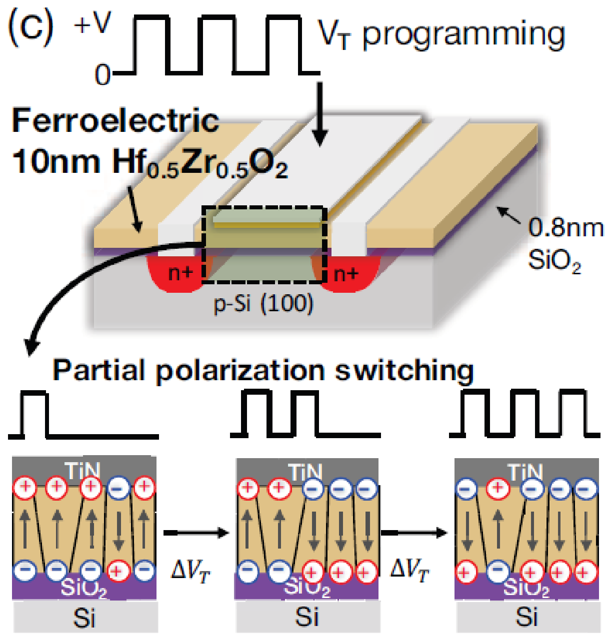
Programmable Resistor based on Ferroelectric Effect

Ferroelectric material:

stores polarization charge due to unique crystal structure







Jerry, IEDM 2017

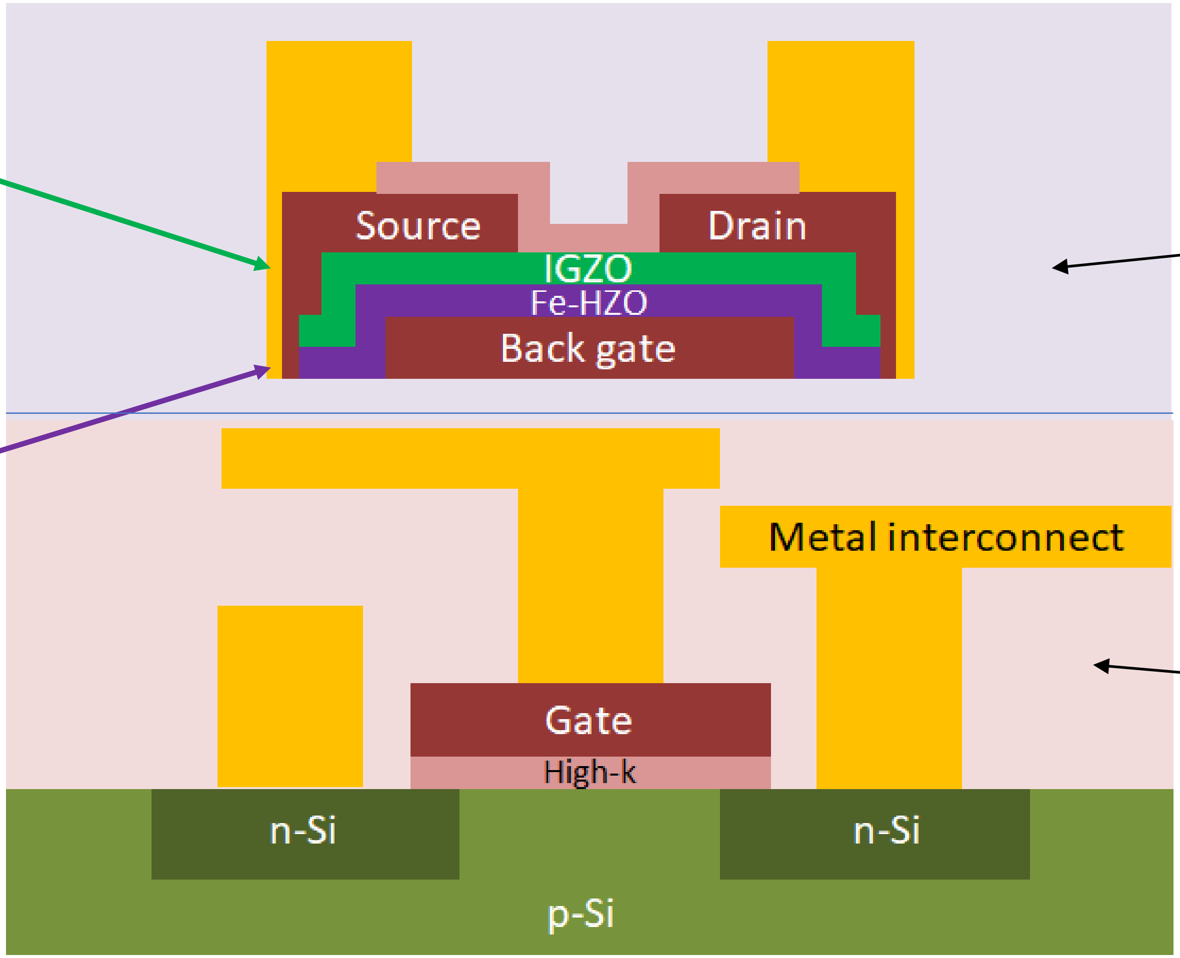
In thin-film with multi-domain structure: partial polarization switching → analog behavior

Our approach: Non-Volatile Thin-Film Ferroelectric MOSFET

Critical requirement: Back-End CMOS compatibility

InGaZnO channel
(T < 400ºC)

Ferroelectric
HfZrO gate
(T ~ 400ºC)

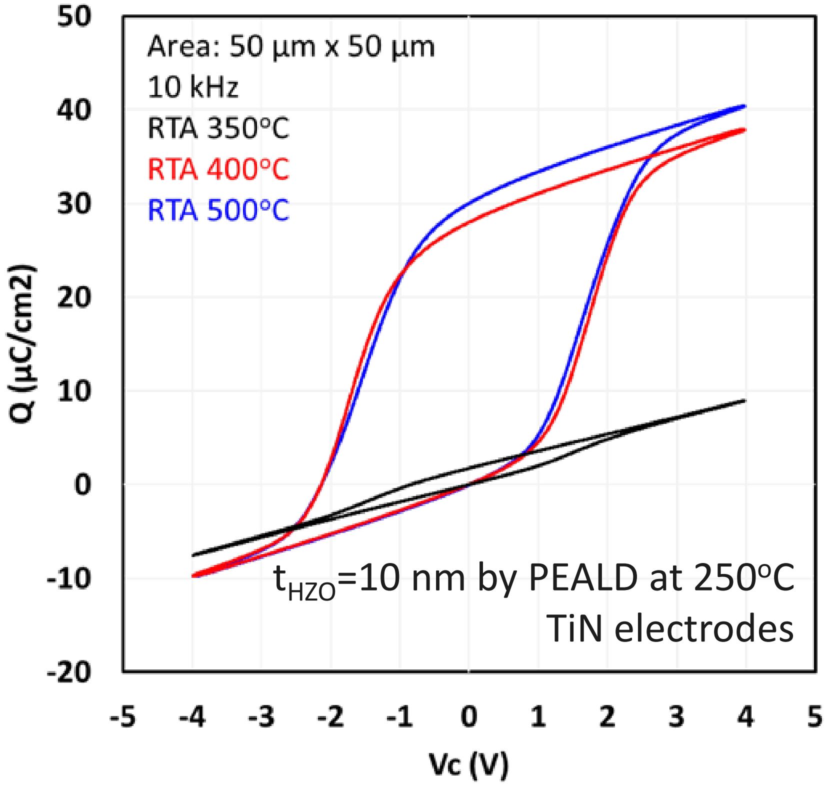


Synapse
fabricated in
CMOS Back-End

CMOS
Front-End

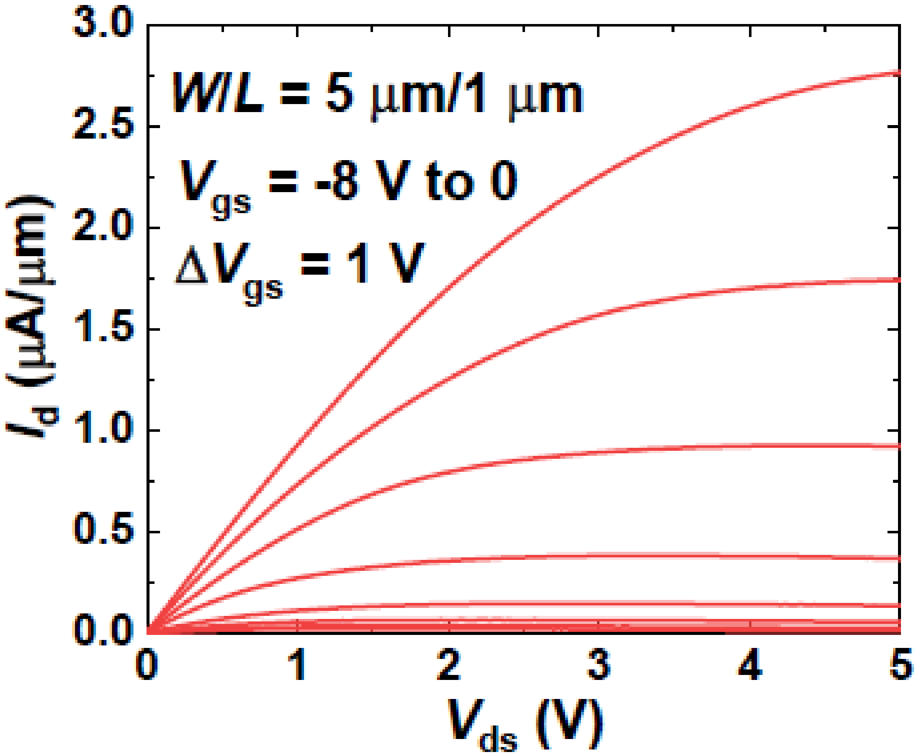
Last Spring:
High-quality HZO films and InGaZnO Transistors @ T≤400^{o}C

HfZrO by 400^{o}C RTA



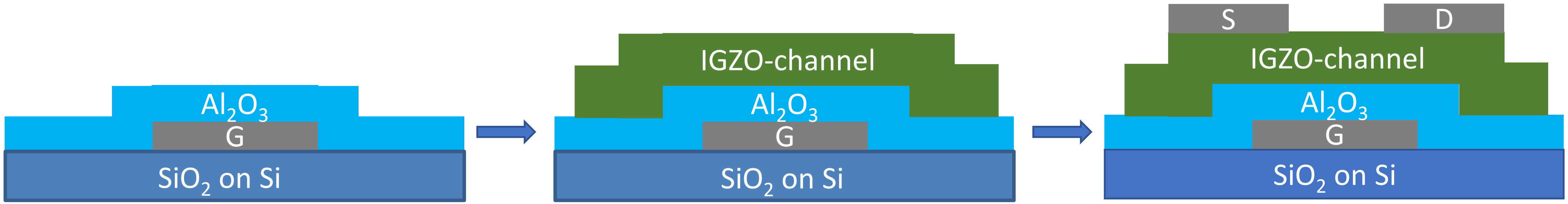
Collaboration with
Ken Cadien (U. Alberta)

InGaZnO Transistor (T_{max}=310^{o}C)



Collaboration with
Pedro Barquinha (U. Nova Lisboa)

Back-gate InGaZnO Thin-Film Transistor



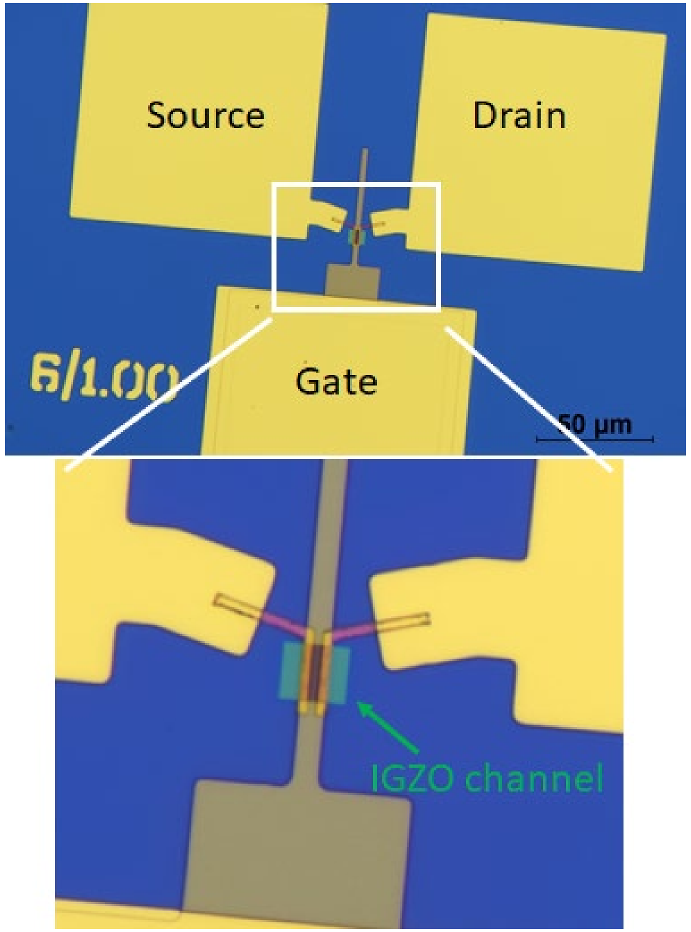
- Ni back-gate lift-off
- Al_2O_3 ALD

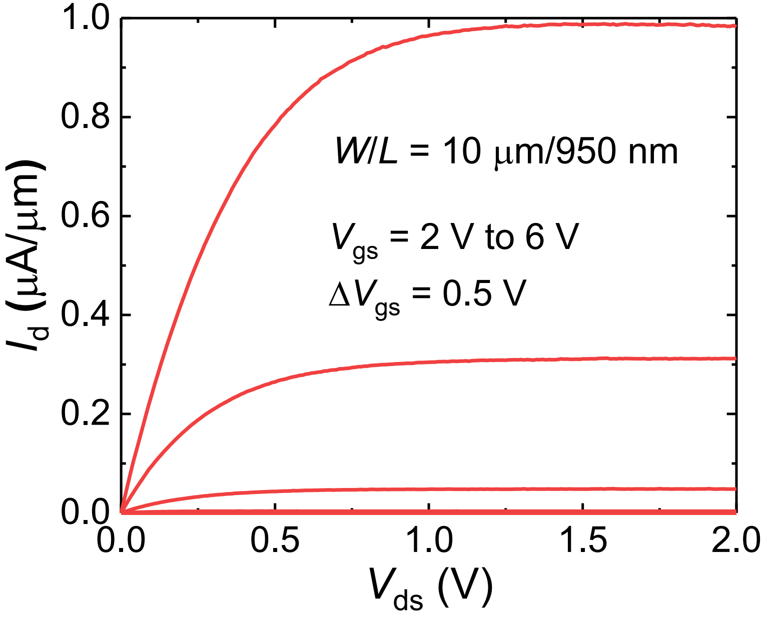
- IGZO sputtering*
- 300^{o}C annealing (air)*
- Mesa wet etch

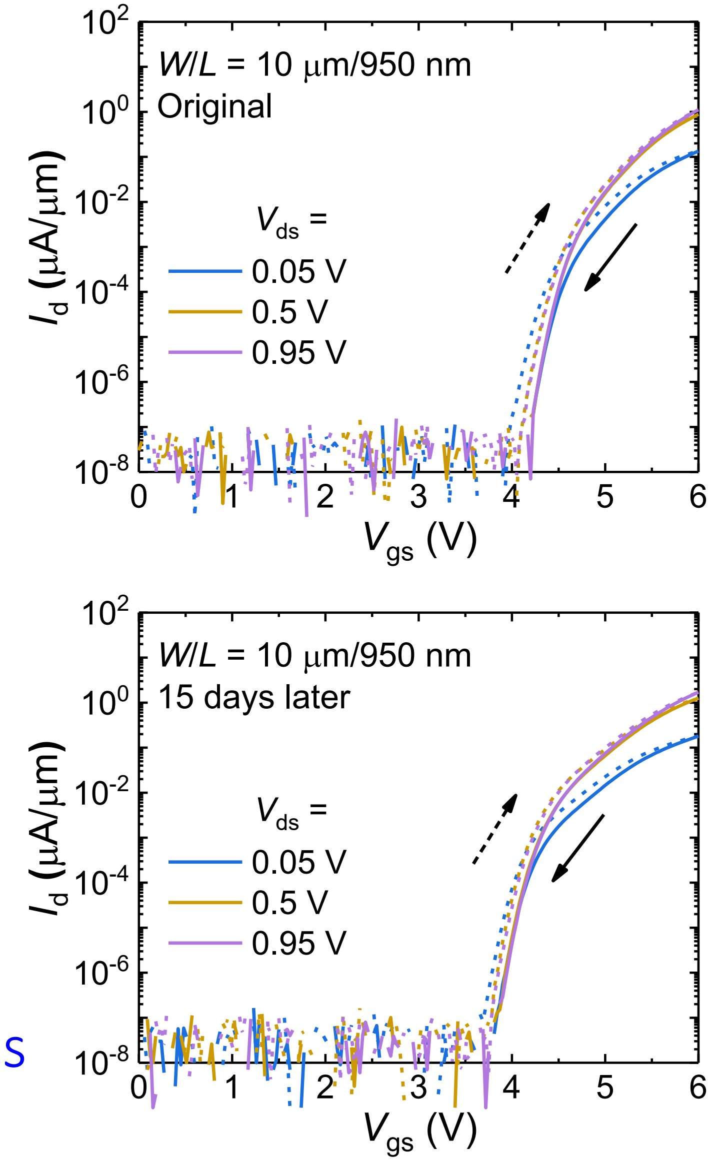
- Source/drain lift-off
- Gate via etching
- Probe pad lift-off
- PMMA passivation

*At University Nova Lisboa

Transistor electrical characteristics



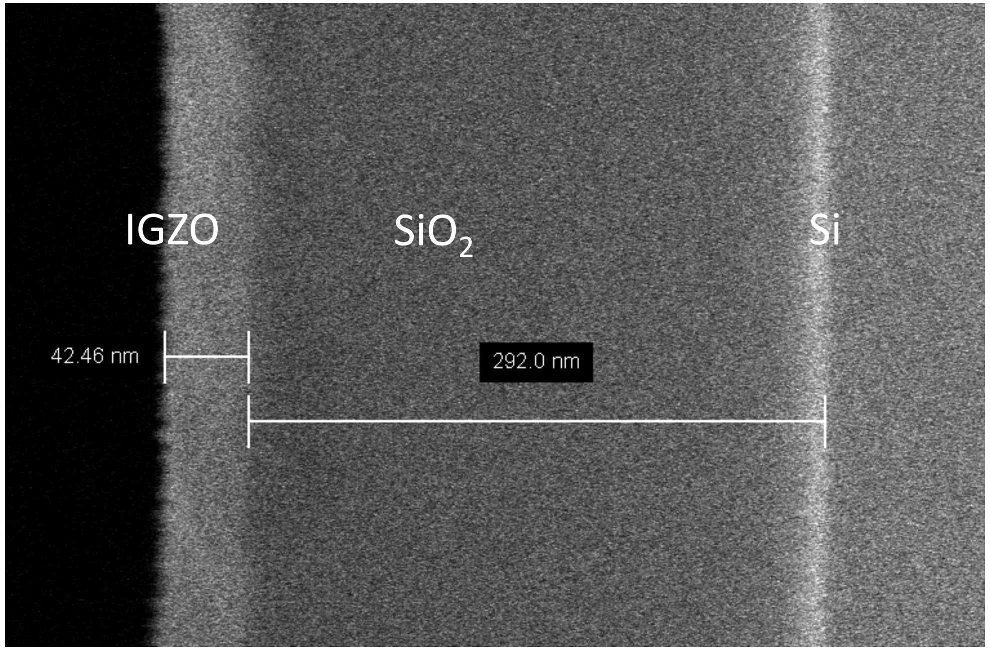


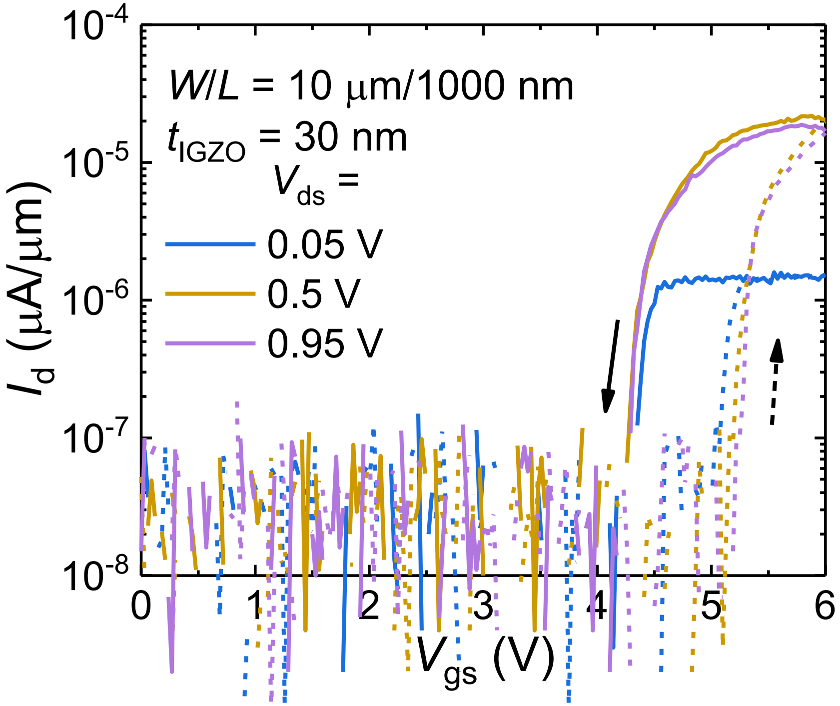


- Well-behaved MOSFET
- Stable electrical characteristics

MIT IGZO by sputtering: first results

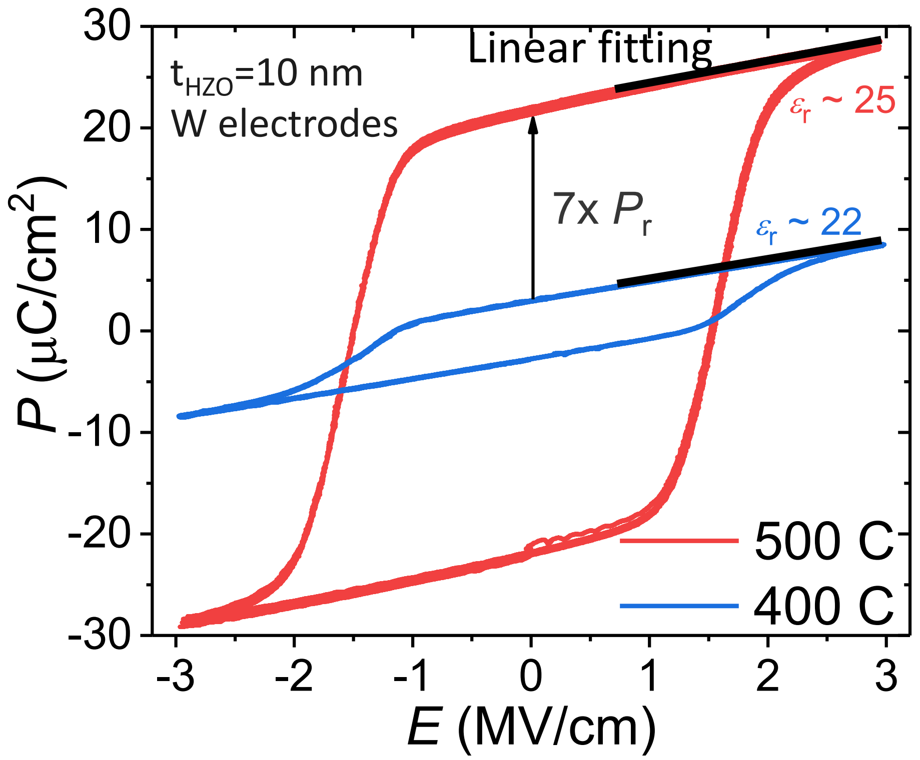
- InGaZnO target, with In:Ga:Zn = 1:1:1
- 20:1 Ar:O_2 flow rate during sputtering
- Linear deposition rate as confirmed from SEM (~0.43 Å/s)
- Device results not optimal, more optimization required





MIT HZO by PE-ALD: first results

HZO by 400°C RTA



- New Arradiance PE-ALD system at MIT
- Precursors: TDMAHf, TDMAZr and O_2 plasma
- Growth sequence: Hf-O-Zr-O
- Growth temperature: 250°C
- Growth rate: 2 Å/supercycle (as desired)
- FE formation temperature: 400, 500°C
- Optimization required

Summary of progress and future work

- Progress:
  - ➢Well behaved back-gate CMOS-compatible IGZO field-effect transistors
  - ➢Demonstration of ferroelectric HZO using PE-ALD at MIT.nano
- Future work:
  - ➢Optimization of IGZO deposition at MIT.nano
  - ➢Enhancement of ferroelectricity in HZO with low thermal budget
  - ➢Integration of ferroelectric HZO into IGZO transistors